Remarks/Arguments

Brief Historical Background

On November 17, 2004 a Final Office Action concerning the above identified Application was mailed to Applicants. On January 18, 2005 an After Final Amendment & Response including a Rule 1.131 Declaration signed by the Applicants and a Declaration by Applicant's Representative in Accordance with MPEP 608.01(p) was filed with the US Patent & Trademark Office. On March 1, 2005 an Advisory Action was mailed to Applicant's Representative by the US Patent & Trademark Office. On April 1, 2005 an Amendment, a further Rule 1.131 Declaration signed by the Applicants, and a Request for Continued Examination was filed. On June 28, 2005 an Office Action was mailed to Applicant's Representative by the US Patent & Trademark Office once again indicating that the Rule 1.131 Declaration was not effective to overcome a Zhang et al reference. On September 28, 2005 a response to the June 28, 2005 Office action was filed together with a further Rule 1.131 Declaration (Declaration under 37 CFR §1.131) signed by the Applicants. On December 16, 2005 another Office Action was mailed to Applicant's representative.

Status and Summary of this response

Claims 1-20 are pending and stand rejected on varying grounds under 35 U.S.C. 103(a).

Claims 1 and 10 have been amended to further clarify the invention. No new matter has been added by any amendment.

In view of the comments below, Applicant respectfully requests that the Examiner enter any proposed amendments, reconsider the present application including claims 1-20, withdraw the rejection of these claims, and move this application to allowance.

a) Applicant notes with appreciation that the DECLARATION filed on September 28, 2005 under 37 CFR 1.131 has overcome the rejections of claims 1-20 based on Zhang et al U.S. Patent 6,560,755 Bl.

b) Claims 1-6 and 8-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, in view of Applicants' Admission.

Claim 1 and claim 10 are independent claims with all other claims in dependent form where each claim of the dependent claims is dependent on the closest lowered numbered one of the independent claims.

This invention is fundamentally different than Michael's approach. A key feature of the present invention as recited by claims 1 or 10 is that it is facilitated by a web interface, e.g. a browser or like interface; rather than being implemented in a computer aided design (CAD) environment, e.g., such as discussed in Michael et al (abstract; page 163, last paragraph). CAD implementations require large overhead, expense and expertise. There are also issues of software maintenance and distribution.

The present invention also allows for a plurality of input parameter data or a range of data, which is not contemplated by Michael et al (see graphical interface definition of claim 1 or claim 10). As noted in an Amendment filed earlier, responsive to a February 26, 2004 Office action, the graphical interface as defined by claim 1 or claim 10 provide a system with the ability to receive multiple values, in possibly different ways (e.g., individually, in a string, in a range, or in a set) for each mismatch input parameter and generate a plurality of mismatch output data based on the overall entered mismatch input data combination. This is valuable because it enables a user to efficiently identify input parameter combinations with favorable (e.g., reasonably reduced) mismatch results.

This is not possible with the scheme of Michael et al. Any results from Michael et al are applicable to a single combination of device size and spacing and electrical bias conditions. See Michael et al, page 163, last paragraph of section III, "Statistical simulation results, shown in Figs. 13 and 14, for the current mirror circuit with constant current bias illustrate the dependencies of device area, separation distance, and bias on the current mismatch variance. Each simulation point on these graphs corresponds to 1000 Monte Carlo simulations using a CAD implementation of the SMOS model." This means that each change in the device geometry (i.e. device area) and/or bias requires an additional execution of the Monte Carlo simulator. Each execution is a complete repetition of a generally known CAD process that may take on the order of an hour to evaluate (i.e., the mismatch on a single pair of devices, for a single geometry and a single bias condition requires: open schematic entry window; input and check schematic; open SPICE simulator window and confirm SPICE model file versions; establish electrical measurements on schematic (this may loop back to modify the schematic, if needed); run a

statistical simulation; parse and interpret results; if results are unsatisfactory go to schematic entry and repeat).

Furthermore in this invention additional features as noted by one or more dependent claims allow for additional efficiency. For example, pre-defined sub-circuit blocks or scenarios are provided to the user in a streamlined web interface, as recited, e.g., in claims 2, 3, 4, 5. By selection of the scenarios listed in claim 4, device connectivity, circuit application, and selection of meaningful results is explicit, thereby stream-lining the interface to the user. This is not possible with the scheme of Michael et al since that approach requires point by point definition of the circuit (by placement and connection of devices), selection of statistical SPICE models, manual simulation and interpretation of the results (see selection discussed above).

Upon submission of the input data, the SPICE simulations are automatically handled by the present invention and the results are evaluated, collated and reported back to the user for easy interpretation and application, which is addressed in varying scope in claims 6, 7, 8, 9. Unlike the Michael et al approach, multiple device geometries and electrical bias conditions can be input to this invention in a single execution (as generally recited in claim 1 and more specifically defined in claim 5). Note that similar observations apply to claims 11-20.

With regard to claims 1-6 and 8-20, the Examiner maintains that "Michael et al. disclose a mismatch modeling tool comprising: the claimed elements including

a graphical interface to said SITMM (Integration of this statistical model into a CAD environment, page 165, left column, paragraph 3).

The Examiner concedes that Michael et al. fails to expressly disclose the format used in the input interface for different scenarios. The Examiner concludes "Nevertheless, Michael et al. have disclosed integrating the model into a CAD environment." As earlier noted, Applicant's invention is unique in that a CAD environment is not contemplated. The Examiner does not address the plurality of input parameter data fields, etc. as recited by the independent claims and which, as discussed above, are a key difference between the present invention and Michael et al.

Next the Examiner mischaracterizes a number of comments in the specification as admissions by the Applicant, e.g., page 5, lines 8-10, "The mismatch tool 10 further comprises the data input and data output interfaces that may be comprised of any data interface method or system"; pages 8-9, changes for added new technologies, for example, make the technology available on the pull down menus, may be accomplished in a variety of methods by those skilled in the art; and at page7, lines 7-9, "the five scenarios above are presented as examples of scenarios popular with those skilled in the art." Applicant fails to see how these comments can be taken out of context and then referred to as Admissions. Even assuming *arguendo* that this was a proper interpretation, these comments do not show or suggest taken alone or together with Michael et al. all of the features (e.g., specifics of the graphical interface) of any one of the claims.

Thus and in view of one or more of the above noted reasons, Michael et al taken alone or together with any other reference does not show or suggest all features of any of the claims and hence these references do not support a rejection of claims 1-6 and 8-20 under §103(a). Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the

rejections of claims 1-6 and 8-20 under 35 U.S.C. 103(a) base on Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, in view of the alleged Applicants' Admission.

c) Claim 7 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, and applicant's admission in view of Hussey (US Patent No. 5,826,269).

Claim 7 is dependent on claim 1 and claim 1 is believed to be allowable over Michael et al., any of Applicant's comments, and Hussey. Hussey and Michael et al. whether taken alone or together do not show or suggest the features that are missing from Michael et al and thus claim 1 and at least by virtue of dependency claim 7 should be allowable over this combination of references. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claim 7 under 35 U.S.C. 103(a) based on Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, and applicant's "admission" in view of Hussey (US Patent No. 5,826,269).

Accordingly, Applicant respectfully submits that the application, as amended, clearly and patentably distinguish over all appropriately cited references of record and as such pending claims 1-20 are to be deemed allowable. Such allowance is hereby earnestly and respectfully

solicited at an early date. If the Examiner has any suggestions or comments or questions, calls are welcomed at the phone number below.

Although it is not anticipated that any fees are due or payable since this response is being timely filed with the allotted three months and no other fees are due or payable, the Commissioner is hereby authorized to charge any fees that may be required to Deposit Account No. **50-3435**.

Respectfully submitted,

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